AMENDMENTS TO THE CLAIMS

1-2. (Canceled).

3. (Currently Amended) ~~The semiconductor integrated circuit according to claim 2,~~ A semiconductor integrated circuit for use in a scan test operation, comprising: at least two blocks to be tested each for performing active functions; an isolation unit for isolating each of said at least two blocks to be tested exclusively from further blocks; and an input terminal for inputting a respective scan clock to each of said at least two blocks, said respective scan clocks input to said at least two blocks each having a phase different from each other, wherein each of said at least two blocks is provided with a Core Wrapper Architecture as said isolation unit.

4. (Original) The semiconductor integrated circuit according to claim 3, wherein a Wrapper register included in said Core Wrapper Architecture is configured to be supplied selectively with one of a scan clock and a system clock for said blocks.

5. (Original) The semiconductor integrated circuit according to claim 4, further comprising: an internal scan chain in each of said at least two blocks, wherein a shift enable signal for said Wrapper register is connected to a scan enable signal for said internal scan chain, a clock for said Wrapper register is synchronous with a scan clock for said internal scan chain in said semiconductor integrated circuit, and serial-in and serial-out terminals of said Wrapper register are each connected to an exterior of said semiconductor integrated circuit, so that an application of scan data from a tester and an observation of results obtained from a test of said application both become feasible.

6. (Original) The semiconductor integrated circuit according to claim 5, further comprising: a logic built-in self test (BIST) in each of said at least two blocks, wherein serial-in and serial-out terminals of said Wrapper register are connected to an output of pseudo-random pattern generators (PRPG), and an input of multiple input serial register (MISR), of said logic BIST, respectively, each in parallel with said internal scan chain between said PRPG and said MISR.

7. (Canceled).

8. (Currently Amended) ~~The semiconductor integrated circuit according to claim 7,~~ A semiconductor integrated circuit capable of performing a scan test, the circuit comprising: at least two blocks to be tested each for performing active functions; an isolation unit for isolating each of said at least two blocks to be tested exclusively from further blocks; and a clock generator for generating a plurality of scan clocks based on a clock input from an exterior controller, a respective scan clock being supplied to each of said at least two blocks, said respective scan clocks supplied to said at least two blocks each having a phase different from each other, wherein each of said at least two blocks is provided with a Core Wrapper Architecture as said isolation unit.

9. (Original) The semiconductor integrated circuit according to claim 8, wherein a Wrapper register included in said Core Wrapper Architecture is configured to be supplied selectively with one of a scan clock and a system clock for said blocks.

10. (Original) The semiconductor integrated circuit according to claim 9, further comprising: an internal scan chain in each of said at least two blocks, wherein a shift enable signal for said Wrapper register is connected to a scan enable signal for said internal scan chain, a clock for said Wrapper register is synchronous with a scan clock for said internal scan chain in said semiconductor integrated circuit, and serial-in and serial-out terminals of said Wrapper register are each connected to an exterior of said semiconductor integrated circuit, so that an application of scan data from a tester and an observation of results obtained from a test of said application both become feasible.

11. (Original) The semiconductor integrated circuit according to claim 10, further comprising: a logic BIST in each of said at least two blocks, wherein serial-in and serial-out terminals of said Wrapper register are connected to an output of PRPG, and an input of MISR, of said logic BIST, respectively, each in parallel with said internal scan chain between said PRPG and said MISR.

12-15. (Canceled).

16. (Currently Amended) ~~The semiconductor integrated circuit according to claim 15,~~ A semiconductor integrated circuit capable of performing a scan test, the circuit comprising: at least two block means to be tested each for performing active functions; means for isolating each of said at least two blocks to be tested exclusively from further block means; and terminal means for inputting a respective scan clock to each of said at least two block means, said respective scan clocks input to said at least two block means each having a phase different from each other, wherein each of said at least two block means is provided with a Core Wrapper Architecture as said means for isolating each of said at least two blocks to be tested.

17. (Original) The semiconductor integrated circuit according to claim 16, wherein a Wrapper register included in said Core Wrapper Architecture is configured to be supplied selectively with one of a scan clock and a system clock for said block means.

18. (Original) The semiconductor integrated circuit according to claim 17, further comprising: internal scan chain means in each of said at least two block means, wherein a shift enable signal for said Wrapper register means is connected to a scan enable signal for said internal scan chain means, a clock for said Wrapper register means is synchronous with a scan clock for said internal scan chain means in said semiconductor integrated circuit means, and serial-in and serial-out terminal means of said Wrapper register means are each connected to an exterior of said semiconductor integrated circuit means, so that an application of scan data from a tester means and an observation of results obtained from a test of said application both become feasible.

19. (Original) The semiconductor integrated circuit according to claim 18, further comprising: logic BIST means in each of said at least two block means, wherein serial-in and serial-out terminals of said Wrapper register means are connected to an output means of PRPG, and an input means of MISR, of said logic BIST means, respectively, each in parallel with said internal scan chain means between said PRPG and said MISR.

20. (Canceled).

21. (Currently Amended) ~~The semiconductor integrated circuit according to claim 20,~~ A semiconductor integrated circuit capable of performing a scan test, the circuit comprising: at least two block means to be tested each for performing active functions; means for isolating each of said at least two block means to be tested exclusively from further block means; and means for generating a plurality of scan clocks based on a clock input from an exterior controller, a respective scan clock to be supplied to each of said at least two block means, said respective scan clocks supplied to said at least two blocks means each having a phase different from each other, wherein each of said at least two block means is provided with a Core Wrapper Architecture as said means for isolating each of said at least two blocks to be tested.

22. (Original) The semiconductor integrated circuit according to claim 21, wherein a Wrapper register included in said Core Wrapper Architecture is configured to be supplied selectively with one of a scan clock and a system clock for said block means.

23. (Original) The semiconductor integrated circuit according to claim 22, further comprising: an internal scan chain means in each of said at least two block means, wherein a shift enable signal for said Wrapper register means is connected to a scan enable signal for said internal scan chain means, a clock for said Wrapper register means is synchronous with a scan clock for said internal scan chain means in said semiconductor integrated circuit means, and serial-in and serial-out terminal means of said Wrapper register means are each connected to an exterior of said semiconductor integrated circuit means, so that an application of scan data from a tester means and an observation of results obtained from a test of said application both become feasible.

24. (Original) The semiconductor integrated circuit according to claim 23, further comprising: a logic BIST in each of said at least two block means, wherein serial-in and serial-out terminals of said Wrapper register means are connected to an output means of PRPG, and an input means of

MISR, of said logic BIST means, respectively, each in parallel with said internal scan chain means between said PRPG and said MISR.

25. (Canceled).

26. (Currently Amended) The semiconductor integrated circuit according to claim ~~2~~ 3, wherein said at least two blocks are isolated from one another and tested in parallel.

27. (Currently Amended) The semiconductor integrated circuit according to claim ~~7~~ 8, wherein said at least two blocks are isolated from one another and tested in parallel.

28. (Canceled).

29. (Currently Amended) The semiconductor integrated circuit according to claim ~~15~~ 16, wherein said at least two block means are isolated from one another and tested in parallel.

30. (Currently Amended) The semiconductor integrated circuit according to claim ~~20~~ 21, wherein said at least two block means are isolated from one another and tested in parallel.